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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

| EXAMINER | |
|---|---|
| PROCTOR, JASON SCOTT | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/063,214 | LEHNER ET AL. | |
| | Examiner | Art Unit | |
| | Jason Proctor | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 10* is/are pending in the application.

4a) Of the above claim(s) *11-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-10 were rejected and claims 11-22 were withdrawn from examination in the office action of 6 April 2006. Applicants' response of 6 July 2006 has amended claims 1-8 and 10; cancelled claim 9; and presented new claims 23-36. Claims 23-36 are withdrawn.

Claims 1-8 and 10 are pending in this application.

Claims 1-8 and 10 are rejected.

### *Prior Art*

The Examiner thanks Applicants for the clarifying remarks submitted in response to the Prior Art section of the previous Office Action. In particular, Applicants submit that:

> Applicants have amended claim 1 to distinctly claim the circuit model of a black box circuit as the model exists in a memory device. **Applicants further submit that the current, voltage, and impedance functions of claim 1 are mathematical functions** used as inputs, outputs, and loads which supply the values necessary to model the response of the real circuit under specified conditions in such a way that the details of the real circuit remain hidden from the user. (page 17, emphasis added)

> The circuit model of the present invention further differs from conventional textbook models, including the models shown in figures 11-5 and 11-7 of the above cited reference [*Floyd –Ex.*] **because it is in an electrical form stored in a memory** and accessed by a computer simulation program (see Lehner abstract, summary, para 70, 78, 102 and Fig. 6-8). (page 24, emphasis added)

These remarks are helpful in understanding the disclosed invention. It must be noted, however, that the term "black box" as claimed does not find antecedent basis or support under 35 U.S.C. § 112, first paragraph, in the application as filed, and use of the phrase has accordingly been rejected as set forth below. Additionally, there are no claim limitations directed to a computer simulation program accessing the circuit model.

Applicants also submit that:

> The circuit model of the claimed invention *uses* models such as miller capacitance, near/far capacitors, resistors, and pi models to derive portions of the black box circuit response during simulation (see Lehner para 12, 24, 51, 65, 87, Fig. 3, and 5-6). For example, a miller capacitance equivalent circuit model may be used to perform one of the capacitance functions recited in claim 1 (see Lehner para. 24, 51, and Fig. 5).

The Examiner disagrees with Applicants' characterization of the claimed invention. There are no pending claims that correspond to these remarks. Please see the Election/Restriction section below. Additionally, the Examiner respectfully requests that when referring to the **claimed invention** that Applicants refer to and specifically cite the **claim language** that allegedly supports the argument.

***Election/Restrictions***

1. Newly submitted claims 23-36 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: A restriction requirement has previously been entered in this application in the Office Action of 20 September 2005, between Invention I "drawn to a circuit model" (claims 1-10) and Invention II "drawn to a method of modeling an integrated circuit" (claims 11-22). Applicants have **elected without traverse** Invention I "drawn to a circuit model." The claims specifying Invention II were withdrawn by Applicants' response of 10 January 2006.

Claims 23-36 are drawn to a method of simulating a "black box" circuit. These claims define an invention generally analogous to Invention II described above. These claims are separate and distinct from Invention I and properly restricted from the application for the same reasons as set forth in the Office Action of 20 September 2005. Further, Applicants have **elected without traverse** to prosecute Invention I in this application.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-36 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### *Drawings*

Replacement drawings were received on 6 July 2006. These drawings are accepted. The previous objections to the drawings have been withdrawn.

### *Specification*

2. The amendments to the specification are objected to because of the following informalities: The amendments, although technically compliant with 37 CFR 1.121, will not be entered because it is apparent that doing so would conflict with Applicants' intentions.

37 CFR 1.121 establishes three methods by which the specification can be amended. These are by replacement specification (37 CFR 1.121(b)(3)), replacement section (37 CFR 1.121(b)(2)), and replacement paragraph (37 CFR 1.121(b)(1)). The present amendments comply with 37 CFR 1.121(b)(1) by identifying paragraphs to be replaced in the specification. However, the Examiner presumes that the inclusion of the various "[...]" symbols in these amendments that Applicants' intention is not to delete and replace these paragraphs, but rather to amend the marked-up portions of the paragraphs as presented. 37 CFR 1.121 makes no provision for this type of amendment to the specification.

Entering these amendments would delete substantial amounts of subject matter. The resulting specification would contain paragraphs that reflect, verbatim, the present amendments to the specification. It is apparent that this is not Applicants' intention; therefore although the amendments are technically compliant with 37 CFR 1.121, they will not be entered.

3. The disclosure is objected to because of the following informalities:

The specification fails to reference FIG. 8 in the "Brief Description of the Drawings." See MPEP 608.01(f).

Paragraph "p31" appears to contain a typographical error in "V2 in the above equation starts is equal to Vout at the beginning of simulation."

Paragraph "p38" appears to contain a typographical error in "In each instance of a selection of pin voltages, The user measures..."

Paragraph "p46" appears to contain a typographical error in "...and may therefore different at every time point."

Paragraph "p79" appears to contain a typographical error in "In the case of simulator's API..."

In paragraph "p80" and after, several references to "code module 25" appear to conflict with the label "circuit module 25" shown in FIG. 7. Some amendments specifically delete the word "circuit" and insert "code," as in the last line of paragraph "p80". Is reference 25 of FIG. 7 a "code module," or a "circuit module," and are these terms synonymous?

Paragraph "p97" has been changed to paragraph "p957", where the intent was presumably "p95".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The previous rejections of claims 1-10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement is withdrawn. Independent claims 1 and 8 have been amended and now specify "a memory" which is described and supported by the specification at paragraph 108 and FIG. 8, referring to a "general-purpose computer" comprising a random access memory and a read-only memory.

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-8 and 10 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claims 1 and 8, as amended, refer to a "black box circuit" which is not described in the application as filed. Applicants' remarks submitted on 6 July 2006 state that:

> The circuit model is shown in Applicant's figures 1-5. Specifically, the circuit model incorporates the functionality of resistors, capacitors, current, and voltage drivers, and is used to model a black box circuit design, thus the circuit model of the present invention is used during simulation so that the details of the real circuit design remain hidden to the user. (See Lehner Figure 1 ckt A, para. 22). The black box circuit is a representation of a proprietary or otherwise confidential circuit (i.e. intellectual property) which is provided to a customer who endeavors to use the circuit either alone or in a larger IC design. Thus, Applicants' claimed invention provides a means for the IP owner to maintain the propriety of the circuit design while enabling the customer to use the design.

Paragraph 22 of the specification describes an "encapsulated (behaviorally equivalent) circuit". The specification contains no reference to a "black box circuit". Whether these terms are completely synonymous is unclear, however employing claim language that finds antecedent basis in the application as filed would circumvent that ambiguity. See also MPEP 608.01(o).

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 and 10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following is an attempt by the Examiner to thoroughly review the claim language for compliance with 35 U.S.C. § 112, second paragraph. The disconnect between the claim terminology and the specification, as well as the several indefinite claims, make it difficult to determine which of the recited limitations are indefinite and which are clear in light of the specification.

Applicants' arguments regarding the rejections under 35 U.S.C. § 112, second paragraph, have been fully considered. The previous rejections under 35 U.S.C. § 112, second paragraph, that are not repeated below have been withdrawn.

The following rejections identify what appear to be clearly indefinite limitations.

Claim 1 recites "a memory for access by a circuit simulation program" and recites several subsequent limitations. The claim recites no limitations that further define "a memory". It is

noted that "a memory" is interpreted as an article of manufacture and should therefore be distinguished from the prior art in terms of its structure. See MPEP 2114. None of the claimed limitations are clearly drawn to structural features of said memory.

Limitations such as "a first and second current function" encompass an enormous breadth and fail to distinguish the invention from the prior art. In the absence of any positively recited claim limitations defining these functions, any integrated circuit device or any circuit model will have some first and second current function, although those functions may amount to no current at all. Similar analysis applies to limitations such as "a first voltage function," "a first, second, and third capacitance function," "an internal impedance function," etc.

The Examiner submits that storing a model of a wire in a computer memory appears to anticipate claim 1. This appears to be completely separate and removed from the disclosure of the invention, and creates substantial ambiguity when attempting to identify the scope of the claimed invention.

6. Similar analysis applies for claim 8. The claim defines "a memory" but recites no structural limitations. The Examiner is aware of no such object as "an impedance" which can be "connected to the output node and ground." To the best of the Examiner's knowledge, impedance is a property, not an object or element with connections.

Applicants' arguments submit that:

> Applicants have amended claim 8 to recite "[...] an internal impedance *value* between the output node and ground." to clarify that impedance value between an output node and ground is required to simulate the black box circuit (see Lehner para 24 and 46, fig. 2 and 5).

The Examiner respectfully traverses this argument as follows.

Claim 8 recites, *inter alia*:

An internal impedance, connected to the output node and ground

The amendments to the claim language to which Applicants' arguments refer have not been found in the claim. Applicants' arguments have been fully considered but have been found unpersuasive.

7. Claim 2 recites "functions of the input node voltage value" which lacks antecedent basis. Neither claim 2 nor the parent claim 1 recites an "input node" or "input node voltage". It is unclear what is meant by functions that "are *subsequently* functions of" other values. This limitation appears to be narrative.

8. Claims 4 and 10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unknown what is meant by "a near capacitor function," "a resistor function," or "a far capacitor function." The Examiner has reviewed the specification and cannot identify where support for this terminology exists.

In response, Applicants argue primarily that:

> Applicants respectfully submit that support for "a near capacitor function", is listed in Applicants' specification paragraphs 86-87, 94, and 100 and is represented by the nomenclature "Cnear_o". Support for a "resistor function" is located in Applicants' specification paragraphs 25, 29-31, 51-52, 59, and 79, and figure 3; and is represented in some instances by the nomenclature Rg, Rload, and R. Support for "a far capacitor function" is located in Applicants' specification paragraphs 86-87, 94, and 100; and is represented by the function "Cfar_o".

The Examiner respectfully traverses this argument as follows.

Referring to the term "a near capacitor function" as representative, Applicants' response does not overcome the grounds of rejection for the following reasons.

The meaning of the term "a near capacitor function" is unknown. When attempting to determine whether the claimed invention is novel and non-obvious, the components of the claimed invention must be clearly defined so that their presence or absence in the prior art can be confirmed. The phrase "a near capacitor function" fails to clearly define the invention because this phrase does not appear to be a well-known term in the art, the plain meaning of these words does not create a definite concept that can be compared with the prior art, and the specification fails to adequately describe what is meant by this phrase.

Applicants' reliance on the specification is appreciated. However, paragraphs 86-87, 94, and 100 do not make any specific reference to "a near capacitor function". The nomenclature "Cnear_o" is described in the computer code of paragraphs 86, 94, and 100 as "float Cnear_o". In the conventions of computer programming, this unambiguously defines a **floating point data value** Cnear_o as a parameter of another function. Therefore, the nomenclature "Cnear_o" does not describe a "near capacitor **function**" because a **floating point data value** and a **function** are separate and distinct concepts.

In summary, it remains unclear how to search the prior art and determine if "a near capacitor function" has been found. Apparently, this limitation requires finding either a floating point data value or a function, despite the claim language. It can be surmised from the phrase that the floating point data value or function is probably related somehow to a capacitance. However, the meaning of a "**near** capacitor function" is entirely unknown. It is unclear how to identify whether a capacitance-related floating point data value or a capacitance-related function is "near". The Examiner maintains that the specification fails to support this claim language with the definiteness required by 35 U.S.C. § 112.

Claims 4 and 10 will not be further treated on their merits.

Applicants' arguments have been fully considered but have been found unpersuasive.

9. Claim 6 recites "the input ... node values" which lacks antecedent basis.

10. Claim 7 recites that "a plurality of the first current functions are arranged in parallel" which renders the claim vague and indefinite. Claim 7 recites "a plurality of the second current functions are ranged in parallel". There is no antecedent basis for a *plurality* of first and second current functions. The meaning of arranging functions in parallel is unknown. Any interpretation of this phrase, in the context of the application, would be speculation.

Claim 7 recites "a portion of a plurality of input node voltage values" which lacks antecedent basis. Claim 7 recites "a portion of a plurality of output node voltage values" which lacks antecedent basis.

In light of the foregoing, claim 7 will not be further treated on the merits.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

***Claim Rejections - 35 USC § 101***

The previous rejections under 35 U.S.C. § 101 of claims 1-10 are withdrawn in response to the amendments to the claims. In particular, the amendments to claims 1 and 8 appear to have clearly identified the statutory category of the invention as an article of manufacture, specifically

"a memory". In light of the specification (paragraphs 108-110; FIG. 8) this is interpreted as a tangible computer-readable storage device.

Applicants' remarks support this interpretation (pages 22-23) and conclude that "the key facts regarding the subject matter of *In re Lowry* are analogous to the facts present in Applicants' Amendment. The claimed invention is a product or article of manufacture.

Applicants submit that:

> Thus claims 1 and 8 are amended are directed to *functional* descriptive material.

The Examiner does not agree with this analysis of the claim language. Claims 1 and 8 describe mathematical functions stored in a memory. Merely storing mathematical functions in a memory does not impart any functionality to a computer system with access to that memory. This is in contrast with, for example, "modules stored in memory that, when executed, configure a computer to compute a first voltage function," which could be a component of functional descriptive material.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-3, 5-6, 8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by "IsSpice4 User's Guide" by Intusoft.

Regarding claims 1-3, 5-6, 8, and 10, Intusoft discloses a computer simulator software, and implicitly "a memory for access by a circuit simulation program" [*"With IsSpice4, Intusoft*

*has added a variety of interactive features, making it the only SPICE 3 simulator with truly interactive performance."* (page 11, second paragraph); *"In addition to porting SPICE 3 to the PC, Macintosh, PowerPC, and Digital Alpha platforms, Intusoft has added enhancements above and beyond the Berkeley version."* (page 11, third paragraph)].

Intusoft discloses that the computer memory comprises a circuit model [*"Code models are a new type of SPICE model, created using a publicly available HDL (Hardware Description Language) based on the C programming language. The code describing the model's behavior is linked to the simulator via an external file (CML.DLL) rather than being bound within the executable program."* (pages 13, last paragraph – page 14)].

Intusoft discloses that the computer memory comprises the various functions [*"You can ask IsSpice4 to stop the simulation when a voltage, current, or a computed device parameter meets a particular condition."* (page 15, second paragraph); *"Real-time viewing and printing of a wide variety of computed device parameters such as device power dissipation, inductor flux, BJT Vbe, and FET transconductance, to name a few."* (page 15, last paragraph); *"Expressions using voltages, currents, computed device parameters and a variety of mathematical functions can be viewed on-screen immediately after the IsSpice4 run, or saved to the output file for viewing in IntuScope."* (page 16, second paragraph)].

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-3, 5-6, 8, and 10 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by US Patent No. 6,718,522 to McBride et al.

Regarding claims 1-3, 5-6, 8, and 10, see FIG. 3, reference 43, and associated description.

Further, McBride discloses a "black box model" (column 1, line 62 – column 2, line 18).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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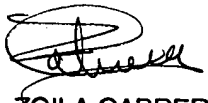

ZOILA CABRERA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

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